Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1	L1 and (vector same (blend$3 or mix$3 or merg$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/14 10:14

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S35	165	345/636.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:28
L45	187	345/636.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:28
S38	25	345/644.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:27
S34	74	345/639.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:27
L44	85	345/639.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:27
L43	30	345/644.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:27
L42	1	(L41) and (vector and key and (blend$4 or merg$4)) and (LUT or "lookup table" or "look up table" or "look-up-table")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:26
L40	9	382/224.ccls. and (vector and key and (LUT or "lookup table" or "look up table" or "look-up-table"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:26
S131	1	(S130) and (vector and key and (blend$4 or merg$4)) and (LUT or "lookup table" or "look up table" or "look-up-table")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:25
S129	7	382/224.ccls. and (vector and key and (LUT or "lookup table" or "look up table" or "look-up-table"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:25
S128	76	382/224.ccls. and (vector and key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:25

L41	176	375/240.22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:25
L39	84	382/224.ccls. and (vector and key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:25
S126	14	(S123 or S124 or S125) and (vector and key and (blend$4 or merg$4)) and (LUT or "lookup table" or "look up table" or "look-up-table")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:24
L38	17	(L35 or L36 or L37) and (vector and key and (blend$4 or merg$4)) and (LUT or "lookup table" or "look up table" or "look-up-table")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:24
L37	1250	375/240.24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:24
L36	428	375/240.23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:24
L35	1426	375/240.01	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:24
S122	57	S121 and (blend$4 or merg$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:23
S119	12	S118 and (blend$4 or merg$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:23
L34	60	L33 and (blend$4 or merg$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:23

L33	194	345/473.ccls. and (key and vector)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:23
L32	13	L30 and (blend$4 or merg$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:23
S118	33	VLIW and (MPEG same vector)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:22
S116	61	S115 and ("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls. or "712"/$.ccls. or "386"/$.ccls. or "724"/$.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:22
L30	35	VLIW and (MPEG same vector)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:22
L29	62	L28 and ("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls. or "712"/$.ccls. or "386"/$.ccls. or "724"/$.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:22
L28	229	L27 and key	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:22
L27	946	vector near7 (blend$4 or merg$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:22
S114	877	vector near7 (blend$4 or merg$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:21
S111	2	345/636.ccls. and ((array or vector or matrix) near7 (alpha or transparen$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:21

S110	2	345/634.ccls. and (vector same blend$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:21
L26	229	L25 and key	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:21
L25	946	vector near7 (blend$4 or merg$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:21
L24	2	345/636.ccls. and ((array or vector or matrix) near7 (alpha or transparen$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:21
L23	2	345/634.ccls. and (vector same blend$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:21
S109	9	382/246.ccls. and ((vector or array or matrix) same (alpha or transparen$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:20
S108	15	712/2.ccls. and (alpha or transparen$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:20
L22	9	382/246.ccls. and ((vector or array or matrix) same (alpha or transparen$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:20
L21	15	712/2.ccls. and (alpha or transparen$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:20
L20	12	712/4.ccls. and (alpha or transparen$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:20
S107	11	712/4.ccls. and (alpha or transparen$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:19

S106	2	345/629.ccls. and (array near7 key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:19
S105	7	345/629.ccls. and (array near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:19
S103	3	345/592.ccls. and (array near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:19
L19	3	345/592.ccls. and (array near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:19
L18	2	345/629.ccls. and (array near7 key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:19
L17	9	345/629.ccls. and (array near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:19
S102	2	345/592.ccls. and (array near7 key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18
S101	6	345/629.ccls. and (matrix same alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18
S100	0	345/629.ccls. and (matrix near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18
S98	1	345/629.ccls. and (vector adj register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18

L16	2	345/592.ccls. and (array near7 key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18
L15	6	345/629.ccls. and (matrix same alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18
L14	0	345/629.ccls. and (matrix near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18
L13	1	345/629.ccls. and (vector adj register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18
L12	4	345/629.ccls. and (vector near3 register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:18
S99	3	345/629.ccls. and (vector near3 register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:17
S97	0	345/629.ccls. and (vector near7 key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:17
L11	0	345/629.ccls. and (vector near7 key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:17
S96	9	345/629.ccls. and (vector near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:16
S95	51	345/592.ccls. and vector	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:16

S94	1	345/592.ccls. and (vector near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:16
S93	0	345/592.ccls. and (vector near7 key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:16
L10	10	345/629.ccls. and (vector near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:16
L9	57	345/592.ccls. and vector	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:16
L8	1	345/592.ccls. and (vector near7 alpha)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:16
L7	0	345/592.ccls. and (vector near7 key)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:16
S90	1	langhi-ronald-gerard.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:14
S89	4	ligon-david.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:14
S88	0	weybrew-steven.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:14
S87	3	weybrew-steven-todd.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:14

L6	2	langhi-ronald-gerard.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:14
L5	5	ligon-david.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:14
L4	0	weybrew-steven.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:14
L3	4	weybrew-steven-todd.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/09/14 10:14
L2	1	L1 and (vector same (blend$3 or mix$3 or merg$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/14 10:14
L1	97	("20030005267"|"4467421"|"4782325"|"5101487"|"5155824"|"5177704"|"5237675"|"5249283"|"5278970"|"5280600"|"5353426"|"5481487"|"5530933"|"5696941"|"5712996"|"5742529"|"5758177"|"5761516"|"5768628"|"5832087"|"5835389"|"5880744"|"5968148"|"5978896"|"6036350"|"6076139"|"6215424"|"6243803"|"6249853"|"6282556"|"6330654"|"6334176"|"6339386"|"6347344"|"6363475"|"6389526"|"6397324"|"6404816"|"6446198"|"6529968"|"6553430"|"6553486"|"6615319"|"6636944"|"6681292"|"6714197"|"6721813"|"6829683").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/09/14 10:13
S130	154	375/240.22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 14:49
S124	374	375/240.23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 14:49

S127	740	382/224.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 14:27
S125	1049	375/240.24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 13:30
S123	1223	375/240.01	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 13:29
S121	188	345/473.ccls. and (key and vector)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 13:11
S120	1016	345/473.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 13:11
S115	217	S114 and key	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:43
S113	5	S112 and vector	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/04/27 10:42
S112	17	(US-20020159632-$).did. or (US-4851912-$ or US-4970595-$ or US-4991014-$ or US-5313566-$ or US-5416529-$ or US-5517437-$ or US-5644365-$ or US-5754186-$ or US-5875355-$ or US-6262778-$ or US-6332030-$ or US-6404923-$ or US-6486888-$ or US-6567096-$ or US-6693643-$ or US-6697076-$).did.	US-PGPUB; USPAT	OR	OFF	2005/04/27 10:30
S37	2	345/636.ccls. and ((array or vector or matrix) near7 (alpha or transparen$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:25

S33	2	345/634.ccls. and (vector same blend$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:25
S43	6	382/246.ccls. and ((vector or array or matrix) same (alpha or transparen$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:24
S46	11	712/2.ccls. and (alpha or transparen$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:18
S47	9	712/4.ccls. and (alpha or transparen$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:03
S19	2	345/592.ccls. and (array near7 alpha)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:01
S18	2	345/592.ccls. and (array near7 key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:01
S17	6	345/629.ccls. and (matrix same alpha)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:00
S16	0	345/629.ccls. and (matrix near7 alpha)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 10:00
S15	1	345/629.ccls. and (vector adj register)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:46
S14	0	345/629.ccls. and (vector near7 key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:46
S13	6	345/629.ccls. and (vector near7 alpha)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:44
S92	890	345/629.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:29

S12	39	345/592.ccls. and vector	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:29
S11	1	345/592.ccls. and (vector near7 alpha)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:29
S10	0	345/592.ccls. and (vector near7 key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:29
S8	712	345/629.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:29
S91	176	345/592.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:28
S9	135	345/592.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:28
S4	0	langhi-ronald-gerard.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:27
S3	0	ligon-david.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:27
S2	1	weybrew-steven-todd.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:27
S1	0	weybrew-steven.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/27 09:27
S75	2	"4991014".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 14:33
S74	126	((replicat$3 or duplicat$3) near7 vector) and ("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 14:33

S73	30139	(replicat$3 or duplicat$3) near7 vector	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 14:21
S58	11	("vector register" or "vector file") and (blend$3 same image)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 14:21
S72	67	("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and "vector file"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 11:42
S71	4	(("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (image near5 (convert$3 or conversion) near5 vector)) and ("video mixing" or "video blending" or "image blending" or "image mixing")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 10:32
S70	1	(("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (image near3 (convert$3 or conversion) near3 vector)) and ("video mixing" or "video blending" or "image blending" or "image mixing")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 10:32
S69	227	("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (image near3 (convert$3 or conversion) near3 vector)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 10:31
S67	3	(("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (vector near5 key)) and ("video mixing" or "video blending" or "image blending" or "image mixing")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 10:31
S68	456	("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (image near5 (convert$3 or conversion) near5 vector)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 10:05
S66	189	("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (vector near5 key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 08:25
S63	1121	("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (vector same (blend$3 or weight))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 08:17
S65	72	((("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (vector same (blend$3 or weight))) and (("look-up" or "lookup" or "look up") adj table)) and (key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 08:02

S64	215	(("345"/$.ccls. or "382"/$.ccls. or "348"/$.ccls.) and (vector same (blend$3 or weight))) and (("look-up" or "lookup" or "look up") adj table)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/27 08:02
S62	3	((US-6693643-$ or US-5754186-$ or US-5875355-$ or US-6567096-$ or US-6486888-$ or US-6697076-$ or US-5517437-$ or US-5416529-$ or US-4851912-$ or US-4970595-$ or US-5313566-$ or US-6262778-$ or US-5644365-$ or US-4991014-$).did. or (US-20020159632-$).did.) and vector	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/05/27 07:59
S61	15	(US-6693643-$ or US-5754186-$ or US-5875355-$ or US-6567096-$ or US-6486888-$ or US-6697076-$ or US-5517437-$ or US-5416529-$ or US-4851912-$ or US-4970595-$ or US-5313566-$ or US-6262778-$ or US-5644365-$ or US-4991014-$).did. or (US-20020159632-$).did.	US-PGPUB; USPAT	OR	OFF	2004/05/27 07:54
S60	125	348/590.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/05/26 14:10
S59	2	"6334176".pn,.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/23 14:43
S57	5	((US-6697076-$ or US-6693643-$ or US-5754186-$ or US-6567096-$ or US-6486888-$ or US-5517437-$ or US-5416529-$ or US-5875355-$ or US-4851912-$ or US-4970595-$ or US-5313566-$).did. or (US-20020159632-$).did.) and register	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/03/23 13:37
S56	12	(US-6697076-$ or US-6693643-$ or US-5754186-$ or US-6567096-$ or US-6486888-$ or US-5517437-$ or US-5416529-$ or US-5875355-$ or US-4851912-$ or US-4970595-$ or US-5313566-$).did. or (US-20020159632-$).did.	US-PGPUB; USPAT	OR	OFF	2004/03/23 13:29
S55	2	"5313566".pn.	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/03/23 11:17

S54	2	"4970595".pn.	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/03/23 11:17
S53	2	"4851912".pn.	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/03/23 11:16
S52	2	"5875355" .pn.	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/03/23 11:00
S51	2	"6549674" .pn.	US-PGPUB; USPAT; DERWENT	OR	OFF	2004/03/23 10:59
S50	117	(image near3 blend$3) and (array same (alpha or transparen$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 14:29
S48	5	(image near3 blend$3) and (vector adj register)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 14:29
S49	5	(image near3 blend$3) and (vector near3 key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 14:27
S44	101	712/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 14:12
S45	76	712/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 14:07
S41	37	382/246.ccls. and (alpha or transparen$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 13:57
S40	316	382/246.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 13:55
S42	3	382/246.ccls. and (alpha or transparen$3) and blend$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 13:50
S39	10	345/644.ccls. and (alpha or transparen$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 13:48

S36	1	345/639.ccls. and ((array or vector or matrix) near7 (alpha or transparen$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 13:32
S32	6	345/634.ccls. and (matrix same blend$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:11
S31	3	345/634.ccls. and (array same blend$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:10
S30	2	345/634.ccls. and (array near7 alpha)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:09
S29	1	345/634.ccls. and (array near7 key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:09
S28	2	345/634.ccls. and (vector near7 key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:09
S27	0	345/634.ccls. and (vector near7 alpha)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:08
S26	314	345/634.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:07
S25	13	345/629.ccls. and (matrix same blend$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:07
S24	11	345/629.ccls. and (vector same blend$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 11:02
S23	13	345/629.ccls. and (array same blend$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 10:57
S22	7	345/629.ccls. and (array same transparenc$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 10:57

S21	2	345/629.ccls. and (array near7 key)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 10:56
S20	3	345/629.ccls. and (array near7 alpha)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 10:54
S7	2	"5875355".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 09:19
S6	2	"5754186".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/22 09:18
S5	0	langhi-ronald.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2004/03/19 14:04

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1 **METHOD FOR EXTRACTING KEY FRAME OF VIDEO SEQUENCE, KEY FRAME EXTRACTING DEVICE FOR VIDEO SEQUENCE, STORAGE MEDIUM AND PROGRAM SOFTWARE**

Inventor: JIN U; LENNON ALISON JOAN **Applicant:** CANON KK

EC: G06F17/30M5; G11B27/28; (+3) **IPC:** H04N7/32; H04N5/92

Publication info: **JP2001258038** - 2001-09-21

2 **SYSTEM AND METHOD FOR USING BITSTREAM INFORMATION TO PROCESS IMAGES FOR USE IN DIGITAL DISPLAY SYSTEMS**

Inventor: MARGULIS NEAL; FOGG CHAD **Applicant:** PIXONICS LLC (US)

EC: G06T1/20; H04N5/14; (+7) **IPC:** G06T1/20

Publication info: **WO0010129** - 2000-02-24

3 **System and method for using bitstream information to process images for use in digital display systems**

Inventor: MARGULIS NEAL (US); FOGG CHAD (US) **Applicant:** PIXONICS LLC (US)

EC: G06T1/20; H04N7/36C; (+1) **IPC:** G06T1/20

Publication info: **US6157396** - 2000-12-05

4 **MOVING PICTURE RETRIEVAL SYSTEM**

Inventor: KATOU KOUKI; ISHIKAWA HIROSHI **Applicant:** FUJITSU LTD

EC: **IPC:** G06F17/30; G06T13/00; (+1)

Publication info: **JP10207897** - 1998-08-07

5 **PICTURE ENCODING METHOD, PICTURE DECODING METHOD AND PICTURE SIGNAL RECORDING MEDIUM**

Inventor: YAGASAKI YOICHI **Applicant:** SONY CORP

EC: G06T9/00T; H04N5/913; (+1) **IPC:** H04N9/804; H04N9/808; (+6)

Publication info: **JP10013858** - 1998-01-16

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vector key table [AND]

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Date of publication of application — e.g.19980401 - 19980405

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blend merge overlay mix OR

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vector key mpeg [AND]

AND

[OR]

AND

[AND]

AND

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1.	2001 - 258038	METHOD FOR EXTRACTING KEY FRAME OF VIDEO SEQUENCE, KEY FRAME EXTRACTING DEVICE FOR VIDEO SEQUENCE, STORAGE MEDIUM AND PROGRAM SOFTWARE
2.	10 - 207897(1998)	MOVING PICTURE RETRIEVAL SYSTEM
3.	10 - 013858(1998)	PICTURE ENCODING METHOD, PICTURE DECODING METHOD AND PICTURE SIGNAL RECORDING MEDIUM

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vector key VLIW AND

AND

OR

AND

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5.	2000 - 207404	METHOD AND DEVICE FOR RETRIEVING DOCUMENT AND RECORD MEDIUM
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19.	05 - 073554(1993)	DOCUMENT OUTPUT DEVICE WITH WRITING ORDER INCORPORATED CHARACTER PATTERN
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23.	03 - 181245(1991)	CONTROL VECTOR TRANSFORMATION DEVICE
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27. 02 - 224068(1990) INFORMATION RETRIEVING SYSTEM
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30. 01 - 246677(1989) SEGMENT LENGTH SIMPLIFIED CALCULATION SYSTEM
31. 63 - 113747(1988) VIRTUAL MEMORY MANAGING DEVICE
32. 63 - 029886(1988) LINEAR GRAPHIC STORING SYSTEM
33. 62 - 295241(1987) MODE PROCESSING CIRCUIT FOR ELECTRONIC APPARATUS
34. 62 - 218835(1987) BALANCE DETECTOR FOR ROTOR
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37. 60 - 120428(1985) CRT DISPLAY CONTROL SYSTEM
38. 60 - 057769(1985) PICTURE RECORDER
39. 58 - 142494(1983) X-Y PLOTTER

Terms used **vector key look up table blend merge overlay** Found **183** of **160,906**

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Relevance scale

1 Three-dimensional medical imaging: algorithms and computer systems

M. R. Stytz, G. Frieder, O. Frieder

December 1991 **ACM Computing Surveys (CSUR)**, Volume 23 Issue 4

Full text available: pdf(7.38 MB) Additional Information: full citation, references, citings, index terms, review

Keywords: Computer graphics, medical imaging, surface rendering, three-dimensional imaging, volume rendering

2 Anti-aliased line drawing using brush extrusion

Turner Whitted

July 1983 **ACM SIGGRAPH Computer Graphics , Proceedings of the 10th annual conference on Computer graphics and interactive techniques**, Volume 17 Issue 3

Full text available: pdf(752.77 KB) Additional Information: full citation, abstract, references, citings, index terms

This algorithm draws lines on a gray-scale raster display by dragging a "brush" along the path of the line. The style of the line is determined by the properties of the brush. An anti-aliasing calculation is performed once for the brush itself and thereafter only a trivial additional operation is needed for each pixel through which the brush is dragged to yield an anti-aliased line. There are few constraints on the size, shape, and attributes of the brush. Lines can b ...

Keywords: Anti-aliasing, Filtering, Line drawing, Painting, Raster display

3 Texture mapping 3D models of real-world scenes

Frederick M. Weinhaus, Venkat Devarajan

December 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 4

Full text available: pdf(1.98 MB) Additional Information: full citation, abstract, references, index terms, review

Texture mapping has become a popular tool in the computer graphics industry in the last few years because it is an easy way to achieve a high degree of realism in computer-generated imagery with very little effort. Over the last decade, texture-mapping techniques have advanced to the point where it is possible to generate real-time perspective simulations of real-world areas by texture mapping every object surface with texture from photographic images of these real-world areas. The techniqu ...

Keywords: anti-aliasing, height field, homogeneous coordinates, image perspective transformation, image warping, multiresolution data, perspective projection, polygons, ray tracing, real-time scene generation, rectification, registration, texture mapping, visual simulators, voxels

4 Hardware acceleration for Window systems

D. Rhoden, C. Wilcox

July 1989 **ACM SIGGRAPH Computer Graphics , Proceedings of the 16th annual conference on Computer graphics and interactive techniques**, Volume 23 Issue 3

Full text available: pdf(1.81 MB) Additional Information: full citation, abstract, references, citings, index terms

Graphics pipelines are quickly evolving to support multitasking workstations. The driving force behind this evolution is the window system, which must provide high performance graphics within multiple windows, while maintaining interactivity. The virtual graphics system presented by [7] provides a clean solution to the problem of context switching graphics hardware between processes, but does not solve all the problems associated with sharing graphics pipelines.The primary difficulty in context ...

5 Status report of the graphic standards planning committee

Computer Graphics staff

August 1979 **ACM SIGGRAPH Computer Graphics**, Volume 13 Issue 3

Full text available: pdf(15.01 MB) Additional Information: full citation, references, citings

6 Pad: an alternative approach to the computer interface

Ken Perlin, David Fox

September 1993 **Proceedings of the 20th annual conference on Computer graphics and interactive techniques**

Full text available: pdf(234.36 KB) Additional Information: full citation, references, citings, index terms

7 A conceptual model of raster graphics systems

James Acquah, James Foley, John Sibert, Patricia Wenner

July 1982 **ACM SIGGRAPH Computer Graphics , Proceedings of the 9th annual conference on Computer graphics and interactive techniques**, Volume 16 Issue 3

Full text available: pdf(672.09 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present a conceptual model of raster graphics systems which integrates, at a suitable level of abstraction, the major features found in both contemporary and anticipated graphics systems. These features are the refresh buffer; the image creation (scan-conversion) system; the single address-space architecture which integrates the address space of the refresh buffer with those of the image creation system and the associated general-purpose computer; the RasterOp or BitBlt ins ...

Keywords: Composition, Look-up table, Pixel-matrix, Raster graphics, RasterOp, Refresh buffer, View

8 Dissertation Abstracts in Computer Graphics

January 1992 **ACM SIGGRAPH Computer Graphics**, Volume 26 Issue 1

Full text available: pdf(2.53 MB) Additional Information: full citation

9 LoD Volume Rendering of FEA Data

Shyh-Kuang Ueng, Yan-Jen Su, Chi-Tang Chang

October 2004 **Proceedings of the conference on Visualization '04**

Full text available: pdf(345.15 KB) Additional Information: full citation, abstract

In this article, a new multiple resolution volume rendering method for Finite Element Analysis (FEA) data is presented. Our method is composed of three stages: At the first

stage, the Gauss points of the FEA cells are calculated. The function values, gradients, diffusions, and influence scopes of the Gauss points are computed. By representing the Gauss points as graph vertices and connecting adjacent Gauss points with edges, an adjacency graph is created. The adjacency graph is used to represent ...

Keywords: Volume rendering, splatting method, level-of-detail, unstructured data, scientific visualization

10 Leo: a system for cost effective 3D shaded graphics

Michael F. Deering, Scott R. Nelson
September 1993 **Proceedings of the 20th annual conference on Computer graphics and interactive techniques**
Full text available: pdf(241.27 KB) Additional Information: full citation, references, citings, index terms

Keywords: 3D graphics hardware, antialiased lines, floating-point microprocessors, gouraud shading, parallel graphics algorithms, rendering

11 Session P9: interactive volume rendering: RTVR: a flexible java library for interactive volume rendering

Lukas Mroz, Helwig Hauser
October 2001 **Proceedings of the conference on Visualization '01**
Full text available: pdf(2.08 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents several distinguishing design features of RTVR - a Java-based library for real-time volume rendering. We describe, how the careful design of data structures, which in our case are based on voxel enumeration, and an intelligent use of look-up tables enable interactive volume rendering even on low-end PC hardware. By assigning voxels to distinct objects within the volume and by using an individual setup and combination of look-up tables for each object, object-aware rendering i ...

Keywords: interactive volume visualization, internet-based visualization, java

12 Designing SoCs for yield improvement: Using embedded FPGAs for SoC yield improvement

Miron Abramovici, Charles Stroud, Marty Emmert
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(200.31 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we show that an embedded FPGA core is an ideal host to implement infrastructure IP for yield improvement in a bus-based SoC. We present methods for testing, diagnosing, and repairing embedded FPGAs, for which complete testability is achieved without any area overhead or performance degradation. We show how an FPGA core can provide embedded testers for other cores in the SoC, so that cores designed to be tested with external vectors can be tested with BIST, and the entire SoC can be ...

13 Mesh parameterization: PolyCube-Maps

Marco Tarini, Kai Hormann, Paolo Cignoni, Claudio Montani
August 2004 **ACM Transactions on Graphics (TOG)**, Volume 23 Issue 3
Full text available: pdf(705.83 KB) mov(22:44 MIN) Additional Information: full citation, abstract, references, index terms

Standard texture mapping of real-world meshes suffers from the presence of seams that need to be introduced in order to avoid excessive distortions and to make the topology of the mesh compatible to the one of the texture domain. In contrast, cube maps provide a mechanism that could be used for seamless texture mapping with low distortion, but only if

the object roughly resembles a cube. We extend this concept to arbitrary meshes by using as texture domain the surface of a *polycube* whose ...

Keywords: *u-v*-mapping, atlas generation, cube maps, surface parameterization, texture mapping

14 Polyhedral subdivision methods for free-form surfaces 

Ahmad H. Nasri

January 1987 **ACM Transactions on Graphics (TOG)**, Volume 6 Issue 1

Full text available: pdf(2.97 MB) Additional Information: full citation, abstract, references, citings, index terms, review

One of the central issues in computer-aided geometric design is the representation of free-form surfaces which are needed for many purposes in engineering and science. Several limitations are imposed on most available surface systems: the rectangularity of the network describing a surface and the manipulation of surfaces without regard to the volume enclosed are examples. Polyhedral subdivision methods suggest themselves as a solution to these problems. Their use, however, is not widespread ...

15 Continuous tone representation of three-dimensional objects illuminated by sky light 

Tomoyuki Nishita, Eihachiro Nakamae

August 1986 **ACM SIGGRAPH Computer Graphics , Proceedings of the 13th annual conference on Computer graphics and interactive techniques**, Volume 20 Issue 4

Full text available: pdf(3.81 MB) Additional Information: full citation, abstract, references, citings, index terms

Natural lighting models to date have been limited to calculation of direct sunlight. However, this paper proposes an improved model for natural lighting calculations that adequately considers both direct sunlight and scattered light caused by clouds and other forms of water vapor in the air. Such indirect natural light is termed skylight and can be an important factor when attempting to render realistic looking images as they might appear under overcast skies.In the proposed natural lighting mod ...

16 Access methods for text 

Chris Faloutsos

March 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 1

Full text available: pdf(2.59 MB) Additional Information: full citation, abstract, references, citings, index terms, review

This paper compares text retrieval methods intended for office systems. The operational requirements of the office environment are discussed, and retrieval methods from database systems and from information retrieval systems are examined. We classify these methods and examine the most interesting representatives of each class. Attempts to speed up retrieval with special purpose hardware are also presented, and issues such as approximate string matching and compression are discussed. A quali ...

17 GI-cube: an architecture for volumetric global illumination and rendering 

Frank Dachille, Arie Kaufman

August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(650.91 KB) Additional Information: full citation, abstract, references, citings, index terms

The power and utility of volume rendering is increased by global illumination. We present a hardware architecture, GI-Cube, designed to accelerate volume rendering, empower volumetric global illumination, and enable a host of ray-based volumetric processing. The algorithm reorders ray processing based on a partitioning of the volume. A cache enables efficient processing of coherent rays within a hardware pipeline. We study the flexibility and performance of this new architecture using both ...

Keywords: hardware accelerator, volume processing, volume rendering, volumetric global

illumination, volumetric ray tracing

18 Combinational logic synthesis for LUT based field programmable gate arrays

Jason Cong, Yuzheng Ding

April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2

Full text available: pdf(628.91 KB) Additional Information: full citation, abstract, references, citings, index terms, review

The increasing popularity of the field programmable gate-array (FPGA) technology has generated a great deal of interest in the algorithmic study and tool development for FPGA-specific design automation problems. The most widely used FPGAs are LUT based FPGAs, in which the basic logic element is a K-input one-output lookup-table (LUT) that can implement any Boolean function of up to K variables. This unique feature of the LUT has brought new challenges to lo ...

Keywords: FPGA, area minimization, computer-aided design of VLSI, decomposition, delay minimization, delay modeling, logic optimization, power minimization, programmable logic, routing, simplification, synthesis, system design, technology mapping

19 An information-theoretic approach to text searching in direct access systems

Ian J. Barton, Susan E. Creasey, Michael F. Lynch, Michael J. Snell

June 1974 **Communications of the ACM**, Volume 17 Issue 6

Full text available: pdf(573.13 KB) Additional Information: full citation, abstract, references, citings, index terms

Using direct access computer files of bibliographic information, an attempt is made to overcome one of the problems often associated with information retrieval, namely, the maintenance and use of large dictionaries, the greater part of which is used only infrequently. A novel method is presented, which maps the hyperbolic frequency distribution of text characteristics onto a rectangular distribution. This is more suited to implementation on storage devices. This method treats tex ...

Keywords: bit vector, character string, direct access, file organization, information retrieval, information theory, text searching

20 A blending model for parametrically defined geometric objects

Ai-Ping Bien, Fuhua Cheng

May 1991 **Proceedings of the first ACM symposium on Solid modeling foundations and CAD/CAM applications**

Full text available: pdf(593.14 KB) Additional Information: full citation, references, citings, index terms

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1 View interpolation for image synthesis

Shenchang Eric Chen, Lance Williams

September 1993 **Proceedings of the 20th annual conference on Computer graphics and interactive techniques**

Full text available: pdf(2.18 MB) Additional Information: full citation, references, citings, index terms

Keywords: image morphing, incremental rendering, interpolation, motion blur, motion compensation, real-time display, shadow, virtual holography, virtual reality

2 Heads, faces, hair: FacEMOTE: qualitative parametric modifiers for facial animations

Meeran Byun, Norman I. Badler

July 2002 **Proceedings of the 2002 ACM SIGGRAPH/Eurographics symposium on Computer animation**

Full text available: pdf(406.87 KB) Additional Information: full citation, abstract, references

We propose a control mechanism for facial expressions by applying a few carefully chosen parametric modifications to pre-existing expression data streams. This approach applies to any facial animation resource expressed in the general MPEG-4 form, whether taken from a library of preset facial expressions, captured from live performance, or entirely manually created. The MPEG-4 Facial Animation Parameters (FAPs) represent a facial expression as a set of parameterized muscle actions, given as inte ...

Keywords: MPEG, animation systems, facial animation

3 Active pages: a computation model for intelligent memory

Mark Oskin, Frederic T. Chong, Timothy Sherwood

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.58 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Microprocessors and memory systems suffer from a growing gap in performance. We introduce *Active Pages,* a computation model which addresses this gap by shifting data-intensive computations to the memory system. An Active Page consists of a page of data and a set of associated functions which can operate upon that data. We describe an implementation of Active Pages on RADram (Reconfigurable Architecture DRAM), a memory system based upon the integration of DRAM and reconfigurable logic. Res ...

4 Configuration cloning: exploiting regularity in dynamic DSP architectures

S. R. Park, W. Burleson
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**
Full text available: pdf(1.72 MB) Additional Information: full citation, references, citings, index terms

5 Multiway FPGA partitioning by fully exploiting design hierarchy
Wen-Jong Fang, Allen C.-H. Wu
January 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 1
Full text available: pdf(130.36 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a new integrated synthesis and partitioning method for multiple-FPGA applications. Our approach bridges the gap between HDL synthesis and physical partitioning by fully exploiting the design hierarchy. We propose a novel multiple-FPGA synthesis and partitioning method which is performed in three phases: (1) fine-grained synthesis, (2) functional-based clustering, and (3) hierarchical set-covering partitioning. This method first synthesizes a design specification in ...

Keywords: fine-grained synthesis, functional clustering, multi-way partitioning, multiple-FPGA synthesis

6 Quality-Driven Proactive Computation Elimination for Power-Aware Multimedia Processing
Shrirang M. Yardi, Michael S. Hsiao, Thomas L. Martin, Dong S. Ha
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**
Full text available: pdf(218.74 KB) Additional Information: full citation, abstract

We present a novel, quality-driven, architectural-level approach that trades-off the output quality to enable power-aware processing of multimedia streams. The error tolerance of multimedia data is exploited to selectively eliminate computation while maintaining a specified output quality. We construct relaxed, synthesized power macro-models for power-hungry units to predict the cycle-accurate power consumption of the input stream on the fly. The macro-models, together with an effective quality ...

7 Enhancing nonverbal human computer interaction with expression recognition
Kostas Karpouzis, Nicolas Tsapatsoulis, Amaryllis Raouzaiou, George Moshovitis, Stefanos Kollias
June 2000 **ACM SIGCAPH Computers and the Physically Handicapped**, Issue 67
Full text available: pdf(624.09 KB) Additional Information: full citation, abstract, references

This paper describes an integrated system for human emotion recognition, which is used to provide feedback about the relevance or impact of the information that is presented to the user. Other techniques in this field extract explicit motion fields from the areas of interest and classify them with the help of templates or training sets; the proposed system, however, compares indication of muscle activation from the human face to data taken from similar actions of a 3-d head model. This compariso ...

8 System partitioning and timing analysis: Design of multi-tasking coprocessor control for Eclipse
Martijn J. Rutten, Jos T. J. van Eijndhoven, Evert-Jan D. Pol
May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**
Full text available: pdf(646.07 KB) Additional Information: full citation, abstract, references, citings, index terms

Eclipse defines a heterogeneous multiprocessor architecture template for data-dependent stream processing. Intended as a scalable and flexible subsystem of forthcoming media-processing systems-on-a-chip, Eclipse combines application configuration flexibility with the

efficiency of function-specific hardware, or coprocessors. To facilitate reuse, Eclipse separates coprocessor *functionality* from generic support that addresses multi-tasking, inter-task synchronization, and data transport. Fi ...

9 Case studies in embedded systems: A fast parallel reed-solomon decoder on a reconfigurable architecture

Arezou Koohi, Nader Bagherzadeh, Chengzi Pan

October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Full text available: pdf(292.18 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a software implementation of a very fast parallel Reed-Solomon decoder on the second generation of MorphoSys reconfigurable computation platform, which is targeting on streamed applications such as multimedia and DSP. Numerous modifications of the first-generation of the architecture have made a scalable computation and communication intensive architecture capable of extracting parallelisms of fine grain in instruction level. Many algorithms and the whole Digital Video Broadc ...

Keywords: Berlekamp algorithm, Chein search, Reed-Solomon codes, SIMD processor, reconfigurable architecture

10 Synchroscalar: A Multiple Clock Domain, Power-Aware, Tile-Based Embedded Processor

John Oliver, Ravishankar Rao, Paul Sultana, Jedidiah Crandall, Erik Czernikowski, Leslie W. Jones IV, Diana Franklin, Venkatesh Akella, Frederic T. Chong

March 2004 **ACM SIGARCH Computer Architecture News , Proceedings of the 31st annual international symposium on Computer architecture ISCA '04**, Volume 32 Issue 2

Full text available: pdf(286.10 KB) Additional Information: full citation, abstract

We present Synchroscalar, a tile-based architecture forembedded processing that is designed to provide the flexibilityof DSPs while approaching the power efficiency ofASICs. We achieve this goal by providing high parallelismand voltage scaling while minimizing control and communicationcosts. Specifically, Synchroscalar uses columnsof processor tiles organized into statically-assignedfrequency-voltage domains to minimize power consumption.Furthermore, while columns use SIMD control to minimizeove ...

11 Interactive three-dimensional holographic displays: seeing the future in depth

Mark Lucente

May 1997 **ACM SIGGRAPH Computer Graphics**, Volume 31 Issue 2

Full text available: pdf(545.74 KB) Additional Information: full citation, abstract, citings, index terms

Computer graphics is confined chiefly to flat images. Images may look three-dimensional (3D), and sometimes create the illusion of 3D when displayed, for example, on a stereoscopic display [16, 13, 12]. Nevertheless, when viewing an image on most display systems, the human visual system (HVS) sees a flat plane of pixels. Volumetric displays can create a 3D computer graphics image, but fail to provide many visual depth cues (e.g. shading texture gradients) and cannot provide the powerful depth cu ...

12 A generic approach for interfacing VRML browsers to various input devices and creating customizable 3D applications

Frank Althoff, Herbert Stocker, Gregor McGlaun, Manfred K. Lang

February 2002 **Proceeding of the seventh international conference on 3D Web technology**

Full text available: pdf(266.82 KB) Additional Information: full citation, abstract, references, citings, index terms

In this work we present a generic architecture for interfacing various input devices to VRML browsers. Concentrating on the aspect of navigation, our system supports the full range of potential input devices from conventional haptic devices like keyboard and mouse over special Virtual-Reality devices like spacemouse and joystick to, as a special feature, semantically higher level input like speech and gesture recognition. The communication

between the individual components of the system is based ...

13 Network processors: a perspective on market requirements, processor architectures and embedded S/W tools

P. Paulin, F. Karim, P. Bromley

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(269.19 KB) Additional Information: full citation, references, citings, index terms

14 Design and Analysis of a Programmable Single-Chip Architecture for DVB-T Base-Band Receiver

Chengzhi Pan, Nader Bagherzadeh, Amir Hosein Kamalizad, Arezou Koohi

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

Full text available: pdf(342.20 KB) Publisher Site Additional Information: full citation, abstract, index terms

This work treats the design and analysis of a programmable (or reconfigurable) DSP-domain-specific architecture called MorphoSys, upon which worldýs first single-chip software solution for DVB-T base-band receiver can be implemented. Based on the first version of MorphoSys, many modifications have been made to improve greatly both computation power and data movement efficiency. Sequential codes and SIMD codes can be parallelized; temporal granularity adjustment boosts up performance up to 4 time ...

15 Computation techniques for FPGAs: An FPGA-based VLIW processor with custom hardware execution

Alex K. Jones, Raymond Hoare, Dara Kusic, Joshua Fazekas, John Foster

February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**

Full text available: pdf(220.52 KB) Additional Information: full citation, abstract, references, index terms

The capability and heterogeneity of new FPGA (Field Programmable Gate Array) devices continues to increase with each new line of devices. Efficiently programming these devices is increasing in difficulty. However, FPGAs continue to be utilized for algorithms traditionally targeted to embedded DSP microprocessors such as signal and image processing applications.This paper presents an architecture that combines VLIW (Very Large Instruction Word) processing with the capability to introduce applicat ...

Keywords: NIOS, VLIW, compiler, kernels, parallelism, synthesis

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1 A code-motion pruning technique for global scheduling

Luiz C. V. Dos Santos, M. J. M. Heijligers, C. A. J. Van Eijk, J. Van Eijnhoven, J. A. G. Jess

January 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 1

Full text available: pdf(293.27 KB) Additional Information: full citation, abstract, references, citings, index terms

In the high-level synthesis of ASICs or in the code generation for ASIPs, the presence of conditionals in the behavioral description represents an obstacle to exploit parallelism. Most existing methods use greedy choices in such a way that the search space is limited by the applied heuristics. For example, they might miss opportunities to optimize across basic block boundaries when treating conditional execution. We propose a constructive method which allows generalized code motions. Schedu ...

Keywords: code generation, code motion, global scheduling, high-level synthesis, speculative execution

2 Configuration cloning: exploiting regularity in dynamic DSP architectures

S. R. Park, W. Burleson

February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**

Full text available: pdf(1.72 MB) Additional Information: full citation, references, citings, index terms

3 Computation techniques for FPGAs: An FPGA-based VLIW processor with custom hardware execution

Alex K. Jones, Raymond Hoare, Dara Kusic, Joshua Fazekas, John Foster

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Full text available: pdf(220.52 KB) Additional Information: full citation, abstract, references, index terms

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Keywords: NIOS, VLIW, compiler, kernels, parallelism, synthesis

PipeRench: a co/processor for streaming multimedia acceleration

Seth Copen Goldstein, Herman Schmit, Matthew Moe, Mihai Budiu, Srihari Cadambi, R. Reed Taylor, Ronald Laufer

May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2

Full text available: pdf(202.69 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

Future computing workloads will emphasize an architecture's ability to perform relatively simple calculations on massive quantities of mixed-width data. This paper describes a novel reconfigurable fabric architecture, PipeRench, optimized to accelerate these types of computations. PipeRench enables fast, robust compilers, supports forward compatibility, and virtualizes configurations, thus removing the fixed size constraint present in other fabrics. For the first time we explore how the bit-widt ...

5 Case studies in embedded systems: A fast parallel reed-solomon decoder on a reconfigurable architecture

Arezou Koohi, Nader Bagherzadeh, Chengzi Pan

October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Full text available: pdf(292.18 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a software implementation of a very fast parallel Reed-Solomon decoder on the second generation of MorphoSys reconfigurable computation platform, which is targeting on streamed applications such as multimedia and DSP. Numerous modifications of the first-generation of the architecture have made a scalable computation and communication intensive architecture capable of extracting parallelisms of fine grain in instruction level. Many algorithms and the whole Digital Video Broadc ...

Keywords: Berlekamp algorithm, Chein search, Reed-Solomon codes, SIMD processor, reconfigurable architecture

6 Quadratic Bezier triangles as drawing primitives

J. Bruijns

August 1998 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.28 MB) Additional Information: full citation, references, citings, index terms

Keywords: 3D graphics rendering, graphics pipeline

7 Synchroscalar: A Multiple Clock Domain, Power-Aware, Tile-Based Embedded Processor

John Oliver, Ravishankar Rao, Paul Sultana, Jedidiah Crandall, Erik Czernikowski, Leslie W. Jones IV, Diana Franklin, Venkatesh Akella, Frederic T. Chong

March 2004 **ACM SIGARCH Computer Architecture News , Proceedings of the 31st annual international symposium on Computer architecture ISCA '04**, Volume 32 Issue 2

Full text available: pdf(286.10 KB) Additional Information: full citation, abstract

We present Synchroscalar, a tile-based architecture forembedded processing that is designed to provide the flexibilityof DSPs while approaching the power efficiency ofASICs. We achieve this goal by providing high parallelismand voltage scaling while minimizing control and communicationcosts. Specifically, Synchroscalar uses columnsof processor tiles organized into statically-assignedfrequency-voltage domains to minimize power consumption.Furthermore, while columns use SIMD control to minimizeove ...

8 Dynamic Functional Unit Assignment for Low Power

Steve Haga, Natasha Reeves, Rajeev Barua, Diana Marculescu

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

Full text available: pdf(175.35 KB) Publisher Site

Additional Information: full citation, abstract, index terms

A hardware method for functional unit assignment is presented, based on the principle that a functional unitýs power consumption is approximated by the switching activity of its inputs. Since computing the Hamming distance of the inputs in hardware is expensive, only a portion of the inputs are examined. Integers often have many identical top bits, due to sign extension, and floating points often have many zeros in the least significant digits, due to the casting of integer values into floating ...

9 Network processors: a perspective on market requirements, processor architectures and embedded S/W tools

P. Paulin, F. Karim, P. Bromley

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(269.19 KB) Additional Information: full citation, references, citings, index terms

10 A high-performance microarchitecture with hardware-programmable functional units

Rahul Razdan, Michael D. Smith

November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture**

Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper explores a novel way to incorporate hardware-programmable resources into a processor microarchitecture to improve the performance of general-purpose applications. Through a coupling of compile-time analysis routines and hardware synthesis tools, we automatically configure a given set of the hardware-programmable functional units (PFUs) and thus augment the base instruction set architecture so that it better meets the instruction set needs of each application. We refer to this new ...

Keywords: automatic instruction set design, compile-time optimization, general-purpose microarchitectures, logic synthesis, programmable logic

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.